CHAPTER 3

MAGNET-TIPPED CHIP FABRICATION AND ATTACHMENT TO ATTONEWTON-SENSITIVITY CANTILEVERS BY FOCUSED ION BEAM MANIPULATION

3.1 Introduction

As discussed in Chapter 2, although the tips fabricated using the integrated magnet-on-cantilever protocol developed by Hickman *et al.* exhibited record-small force sensitivity near a surface, their fabrication was problematic [81]. The nanomagnets were damaged extensively by processing incompatibilities during the thirty-eight steps of fabrication, resulting in extremely low yields. Scanning electron microscopy (SEM) imaging indicated that less than 1% of the magnets remained intact after processing; the rest of the magnets were either physically absent after processing or were damaged and unusable, as shown in Figure 2.2.

In order to conduct high resolution MRFM experiments, process yields had to be greatly improved and magnet damage had to be reduced, particularly at the leading edge where the force gradient acting on the sample spins is greatest. To this end, a high-yield method for fabricating overhanging nanomagnets on micrometer-scale silicon chips and serially attaching them to attonewton-sensitivity cantilevers has been developed. This approach made it possible to reduce the processing time for nanomagnet fabrication from approximately two weeks (see Section 2.3) to just four days, and it completely decoupled the fabrication of the nanomagnets, which are particularly susceptible to heating and chemical damage, from the fabrication of the cantilevers, which involves multiple high-temperature processing steps. The process was first successfully demonstrated for nickel nanomagnets; process modifications have also enabled the fabrication of cobalt nanomagnets, which have saturated magnetic moments that are three times higher than is observed for nickel.

The high-yield fabrication protocol involves a combination of batch- and serial-fabrication techniques. The overhanging nanomagnets were batch-fabricated on silicon microchips. These microchips were released prior to deposition of the nanomagnets so that the chips could be analyzed after any post-deposition processing step. To obtain nanomagnets on cantilevers, the magnet-tipped chips were serially attached to separately-fabricated attonewton-sensitivity silicon cantilevers using focused ion beam (FIB) manipulation. FIB lift-out and milling is routinely used to image sample cross-sections [127, 128] and to prepare transmission electron microscopy (TEM) samples [129–132]. Here we show that the ability of FIB to mill, transfer, and adhere samples with microscale precision makes it an ideal tool for lifting out the magnet-tipped chips and adhering them to the leading edges of cantilevers.

In addition to the fabrication details provided in the subsequent sections, thorough procedures for fabricating the magnet-tipped chips and for conducting the FIB attachment protocol are provided in Appendix A and Appendix B, respectively. A step-by-step procedure for fabricating blank cantilevers can be found in Appendix A of Ref. 91, starting with Section A.5.

3.2 Nickel Nanomagnet-Tipped Chip Fabrication Protocol

Overhanging nanomagnet-tipped silicon chips were fabricated from 100 mm diameter silicon-on-insulator (SOI) wafers having a device silicon thickness of 340 nm, a buried oxide (BOX) thickness of 400 nm, and a silicon handle wafer thickness of 500 µm. The device silicon resistivity was 14 to 22 Ω cm, corresponding to a boron dopant concentration of 6 to 9 × 10^{14} cm^{-3}.

Alignment Marks. Lift-off alignment marks for the three subsequent electron beam (e-beam) lithography steps were defined in a bilayer of 50 nm of 950,000 molecular weight

(MW) (poly)methylmethacrylate (PMMA) on top of 550 nm of 495,000 MW PMMA, and were patterned using either a JEOL JBX9300FS (at 2 nA) or a JEOL JBX6300FS 100 kV (at 1 nA) e-beam lithography system. The marks were deposited by e-beam evaporation (CVC products SC 4500 evaporator) and consisted of a 5 nm chromium or titanium adhesion layer with 100 nm of platinum. All materials were deposited at a rate of approximately 2.0 Å/sec. The resist and excess metal were removed by sonication in a 1:1 (v/v) solution of methylene chloride (CH_2Cl_2) and acetone. Separate sets of global alignment marks, which were used for global positioning and rotation of the wafer, and local marks, which were needed to determine the precise center of each die of magnet-tipped chips, were patterned for each of the three subsequent layers; a fourth set of marks was also patterned as a spare set. It was necessary to fabricate individual sets of alignment marks for each layer because the marks were often damaged while manually locating them in SEM mode prior to exposure. In SEM mode, all of the resist over the imaged region, was exposed. The exposed mark was then damaged by the subsequent processing steps. These processed areas, in which either the silicon was etched or magnetic material was deposited over the mark (Figure 3.1), often lost the contrast needed for e-beam alignment and were unusable for subsequent alignments.

Chip Design and Release. Slits to define rectangular chip bodies, along with support tethers halfway along the chip length to prevent post-release stiction, were defined in approximately 700 nm of 495,000 MW PMMA and patterned by e-beam lithography. These "etch slits" can be seen in Figure 3.2(a).[1] The device-layer silicon was etched in sulfur hexafluoride and oxygen (SF_6:O_2; Oxford Instruments Plasmalab 80), and the resist was subsequently stripped by sonication in a 1:1 (v/v) solution of methylene chloride and acetone. The chips were released by wet etching of the BOX layer in 6:1 buffered oxide etch (BOE), followed by soaking the wafer in a water bath and spin drying.

[1]Figures 3.2, 3.5, 3.6, and 3.12(c) reprinted with permission from J. G. Longenecker *et al.*, J. Vac. Sci. Technol. B **29**, 032001 (2011). Copyright 2011, American Vacuum Society.

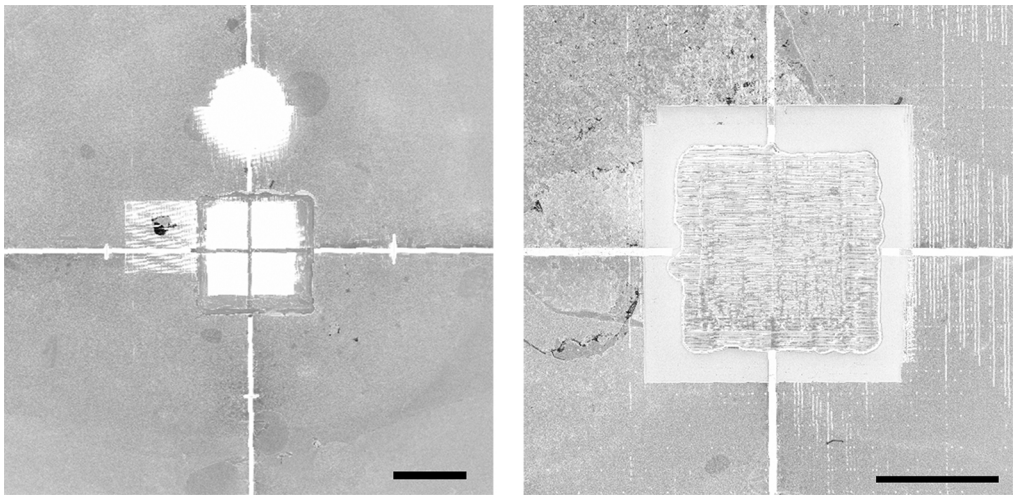

Figure 3.1: Damaged e-beam lithography alignment marks. When an alignment mark was located manually in SEM mode, the resist over the alignment mark was exposed, and the mark was damaged by the subsequent processing steps. The marks were damaged either by SF_6:O_2 plasma etching of the device silicon layer surrounding an exposed alignment mark or by the alignment mark being covered by magnetic material during the magnet definition processing step. Both scale bars represent 50 µm.

Nanomagnet Deposition. Nickel nanomagnets with widths of 70 nm, 110 nm, and 220 nm were patterned by e-beam lithography in a bilayer of 50 nm of 950,000 MW PMMA on 550 nm of 495,000 MW PMMA. The magnets were deposited by e-beam evaporation; a 5 nm thick chromium[2] adhesion layer was deposited prior to evaporating the 100 nm thick magnets. Chromium was deposited at a rate of 2.0 Å/s, and nickel was deposited at a rate of 2.5 Å/s. After a waiting period to allow the chamber to cool to room temperature, the wafer was unloaded and the resist and excess metal were removed by sonication in a 1:1 solution of methylene chloride and acetone, followed by spin drying. A nanomagnet deposited on a suspended silicon chip is shown in Figure 3.2(b). To protect against post-processing oxidation, some samples were coated with approximately 6 nm of alumina prior to resist removal. The alumina was prepared via atomic layer deposition (ALD; Oxford FlexAL) using trimethlyaluminum and plasma oxygen precursors at 110°C [115, 116].

[2]It has subsequently been determined that titanium is a better choice for an adhesion layer, since chromium is antiferromagnetic [133].

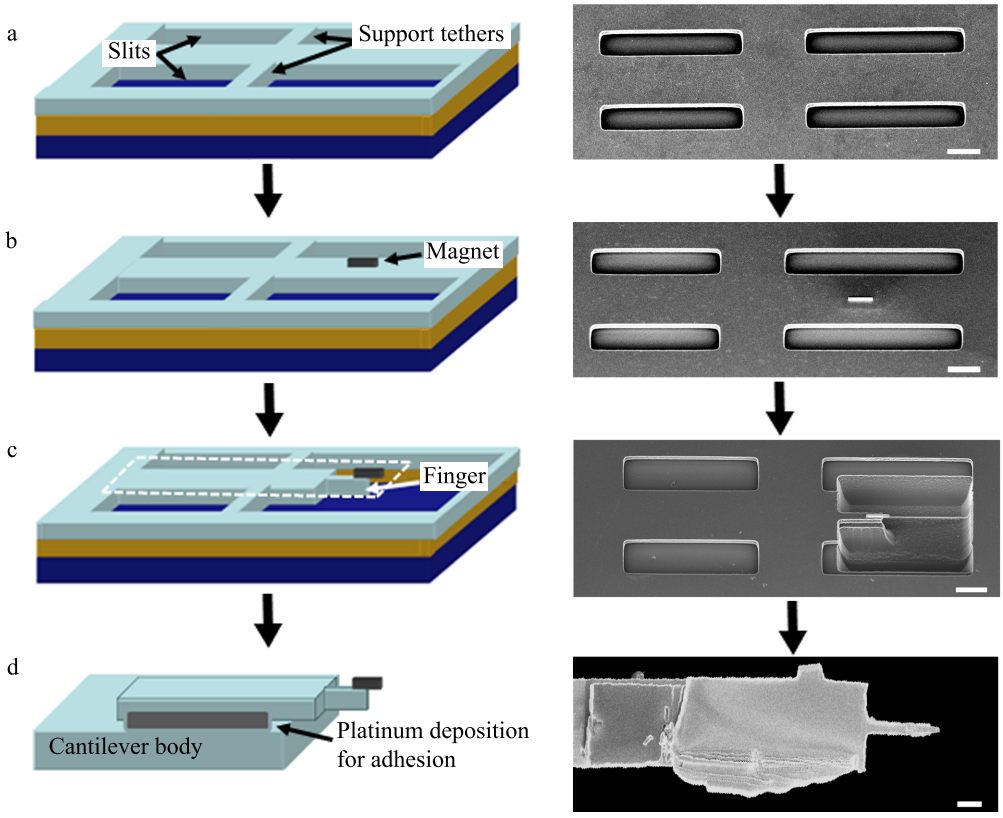

Figure 3.2: Process flow schematics (left) and corresponding SEM images (right) at key steps in the process used to fabricate overhanging magnet-tipped silicon chips and attach the chips to cantilevers. The layers in the schematics correspond to the nickel magnet (black), device silicon (light blue), buried silicon dioxide (yellow), handle silicon (dark blue), and ion-beam deposited platinum for adhesion of the chip to the cantilever (gray). The magnet-tipped chips were fabricated by (a) etch slit definition and chip release, (b) magnet deposition, and (c) definition of silicon leading-edge "fingers". Note that because the chips were released prior to the silicon finger definition, the handle-wafer silicon was also etched, creating deep U-shaped craters as shown in the SEM in panel (c). To attach the chip to a cantilever, the portion of the chip inside the dashed line in the schematic in panel (c) was lifted out and attached to the leading edge of the cantilever (see Figure 3.5), resulting in the magnet-tipped chip-on-cantilever shown in panel (d). All scale bars represent 2 µm.

Silicon Underetch of U-Shaped Etch Pits. In order to achieve overhanging magnets, as shown in Figure 3.2(c) and Figure 3.3, the silicon under the nanomagnets was removed by defining U-shaped "etch pits" in front of the nanomagnets. The etch pits were patterned by e-beam lithography in approximately 700 nm of 495,000 MW PMMA and were isotropically etched using SF_6:O_2 plasma. The position of the U-shaped pits and the etch time were carefully calibrated so that the nanomagnets extended past the silicon leading edge by 300 to 400 nm (Figure 3.3(c-f)). Because of the design of the U-shaped holes, silicon "fingers" were also defined at the leading edges of the chips that were 2 to 3 µm long and 1 µm wide. The resist was removed by sonication in a 1:1 solution of methylene chloride and acetone, followed by spin drying.

Overall, the magnet-tipped silicon chip fabrication protocol required 17 steps and could be completed within four days of processing time. The process is currently designed to produce four dies with 100 chips each per wafer, but could be redesigned to produce thousands of chips per wafer. The factor of three improvement in processing time, when compared to the integrated magnet-on-cantilever fabrication protocol of Ref. 81, enables the rapid prototyping of new chip designs, magnet dimensions, and magnetic materials.

3.3 Summary of Blank Cantilever Fabrication

Attonewton-sensitivity silicon cantilevers that were either intentionally magnet-free (also known as "blank" cantilevers) or were from failed magnet-on-cantilever trials (see Section 2.3), with the metal-tipped fingers milled away, have been used for magnet-tipped chip attachment (Figure 3.4). The scheme for the batch fabrication of these cantilevers is similar to previous protocols [66, 68, 81]. Currently 21 dies with 10 cantilevers each, totaling 210 cantilevers, are prepared per wafer.

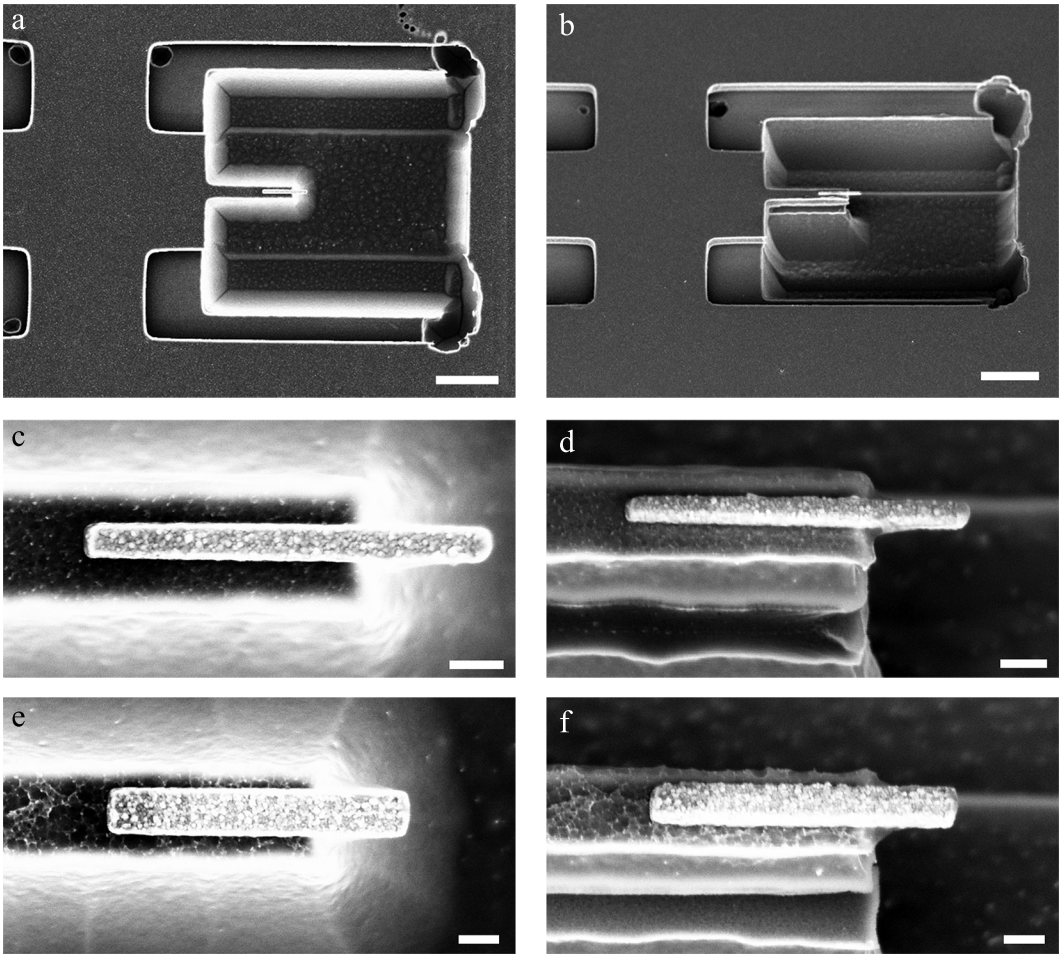

Figure 3.3: Top-down (left column) and side-on (right column) SEM images of the leading edges of magnet-tipped chips and magnified views of overhanging nickel nanomagnets. (a-b) Views of the leading edges of magnet-tipped chips. The deep pit etched into the silicon resulted from etching U-shaped holes into the suspended device silicon layer; since there was air instead of a BOX etch-stop layer between the device silicon and underlying handle silicon layers, a by-product of etching the device silicon layer to create the overhanging magnet and reduced-width silicon finger was that the observed pit was also etched into the handle silicon layer. (c-d) A 115 nm wide nickel nanomagnet that extended past the leading edge of the silicon chip by 380 nm. (e-f) A 225 nm wide nickel nanomagnet that extended past the leading edge of the chip by 400 nm. The scale bars in (a) and (b) represent 2 µm, and the scale bars in (c-f) represent 200 nm.

The cantilevers were fabricated from silicon-on-insulator (SOI) wafers identical to those used to prepare the nanomagnet-tipped silicon chips (Section 3.2). Cantilever bodies that were 195 µm long and 4 µm wide, as shown in Figure 3.4(b), were patterned in the single-crystal device silicon layer by photolithography using an Autostep 200 5× reduction wafer exposure tool, followed by an SF_6:O_2 isotropic plasma etch. In order to protect against scratching of the cantilevers during back side processing, the front of the wafer was coated with 1.6 µm of low-stress plasma enhanced chemical vapor deposition (PECVD) SiO_2 using a GSI PECVD system. The back of the wafer was coated with 2 µm of PECVD SiO_2 for an etch mask. Windows in the back side of the wafer were aligned underneath the cantilever bodies and patterned by contact photolithography; the alignment marks for this front-to-back alignment were patterned during the cantilever body definition step. The PECVD SiO_2 was etched using a CHF_3 reactive ion etch, and the underlying silicon handle wafer was etched by Bosch through-wafer processing using the procedure described in Appendix A.11 of Ref. 91. The Bosch etch both created windows in the silicon under the cantilevers and defined cantilever handle dies (Figure 3.4(a)), which are necessary for the transport and handling of the cantilevers. The resist on the back side of the wafer was removed partway through the Bosch etch, leaving the back side SiO_2 as the only etch mask during the etching of the final 100 µm of handle wafer silicon. The cantilevers were released in BOE, and critical point drying (CPD) was used to to prevent stiction or curling of the cantilevers.

The 195 µm long cantilevers fabricated using this method have had resonance frequencies $f_c \approx 9000$ Hz, spring constants of approximately $k = 0.75$ mN m^{-1}, and intrinsic quality factors ranging from $Q = 40,000$ to $Q = 100,000$ in high vacuum and at 4 K. Parameters that contribute to the cantilever quality factor are not fully understood, but studies have shown that Q can be strongly altered by surface effects [66, 80]. For our cantilevers, a second factor that can affect Q is a "shelf" of device layer silicon at the base of the cantilever that is caused by the back side through-wafer Bosch etching of the 500 µm thick silicon handle

wafer layer. Bosch etching is a process by which an isotropic plasma process is converted into an anisotropic method for etching deep into silicon by alternating between steps that (1) isotropically etch a shallow trench into the silicon layer, (2) deposit a protective fluorocarbon layer onto the side walls and base of the silicon trench, and (3) directionally etch the base of the trench to remove the fluorocarbon polymer and further etch the silicon [102]. Bosch etching results in mostly-directional etching of silicon, but the silicon trench does broaden with depth. In our case, this broadening led to tapering back of the silicon device layer as it was etched from the back side of the wafer, which exposed more than 50 µm of the device silicon layer of the cantilever handle die; this exposed shelf is highlighted by the arrow in Figure 3.4(a). Because this unsupported shelf is only 340 nm thick, the shelf bends when the cantilever oscillates. We have observed that the cantilever Q is greatly damped if there are any cracks in this shelf.

3.4 Focused Ion Beam Lift-Out and Attachment to Cantilevers

FIB processing was conducted using a dual-beam FEI Strata 400 STEM FIB system with ion beam and e-beam imaging, ion beam milling, and platinum deposition capabilities. The dual-beam FIB also was equipped with a probe needle with a 1 µm diameter tip for transferring samples. A schematic of the lift-out and attachment process is shown in Figure 3.5. In order to prevent gallium ion implantation, the magnets always remained out-of-view of the ion beam. All ion beam processing was done at 30 kV with a nominal ion beam current of 28 pA. Exposure of the magnets to the ion beam was limited to less than three seconds of total exposure, all at low resolution ($< 650\times$); the total ion dose experienced by the magnetic material was less than 0.22 µC cm^2.

To attach a magnet-tipped silicon chip to the probe needle, the tip of the needle was

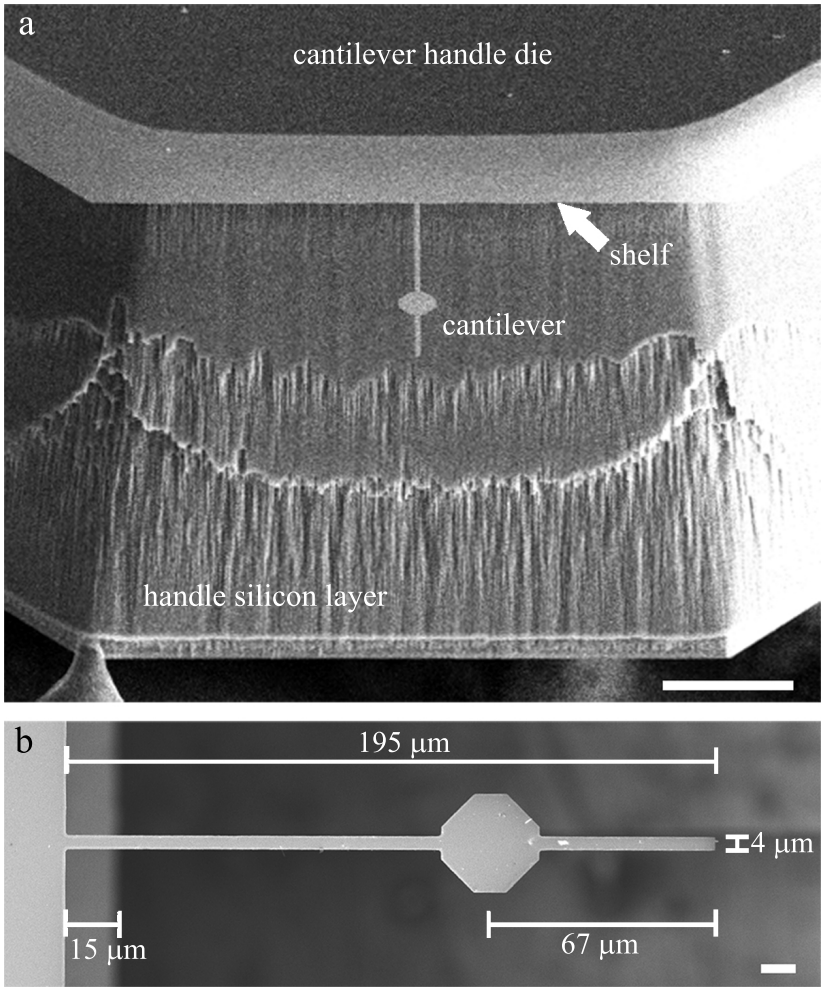

Figure 3.4: SEM images of 195 µm long cantilevers with the components and dimensions of the cantilever chips labeled. (a) Angled front-on image of a cantilever attached to its cantilever handle die. The tapering of the handle die side wall leads to a "shelf" of unsupported handle wafer at the cantilever leading edge; the portion of the handle die that is connected to the underlying handle silicon layer is shown as dark gray in the SEM image, and the unsupported shelf (indicated with the arrow) is much lighter in color. Additional nonuniformities caused by the Bosch etch can be seen in the handle silicon layer. (b) Image of a blank cantilever. The length and width of the cantilever, as well as the distance from the cantilever leading edge to the center of the cantilever pad used for interferometric detection of the cantilever motion, are labeled. The base of the cantilever handle die is observed to protrude past the front of the cantilever handle die shelf by 15 µm. The scale bar in (a) represents 100 µm and the scale bar in (b) represents 10 µm.

brought into light contact with the chip surface approximately 5 µm from the base of the chip. The needle was adhered to the silicon chip using platinum deposition to join the two components (Figure 3.5(a)). For all adhesions, approximately 1 µm of platinum was deposited by ion-beam-induced decomposition of methylcyclopentadienyl(trimethyl)platinum(IV) precursor gas. After adhesion of the chip to the needle, the chip base and support tethers were milled (Figure 3.5(b)) and the chip was gently raised from the substrate and moved near the cantilever's leading edge.

Before the chip was brought into contact with the cantilever, the chip and cantilever were aligned horizontally by rotating the stage (and mounted cantilever) as needed. The chip was softly brought into contact with the cantilever (Figure 3.5(c)). Since the cantilevers tend to bend downward at a slight angle, the probe was retracted slightly to pull the cantilever upwards and improve vertical alignment between the chip and the cantilever. Once the vertical alignment was confirmed, platinum was deposited on the sides of the chip and cantilever to facilitate adhesion (Figure 3.5(d)). The probe tip was milled, and the probe was lifted away from the cantilever (Figure 3.5(e)). Additional platinum-deposited contacts were added to the side and top of the cantilever. A completed chip mounted on a cantilever is shown in Figure 3.5(f).

3.5 Nanomagnet-Tipped Chip Process Yield

Yields were estimated for the fabrication of the magnet-tipped chip bodies, cantilevers, and FIB attachment procedure. By analyzing thirteen magnet-tipped silicon chip dies, with each die containing 100 individual magnet-tipped silicon chips, an average magnet-tipped chip body yield was estimated to be $94.2\% \pm 6.0\%$. It was determined that in order to achieve this high yield, the width of the slits, the width of the support tethers, and the length of the

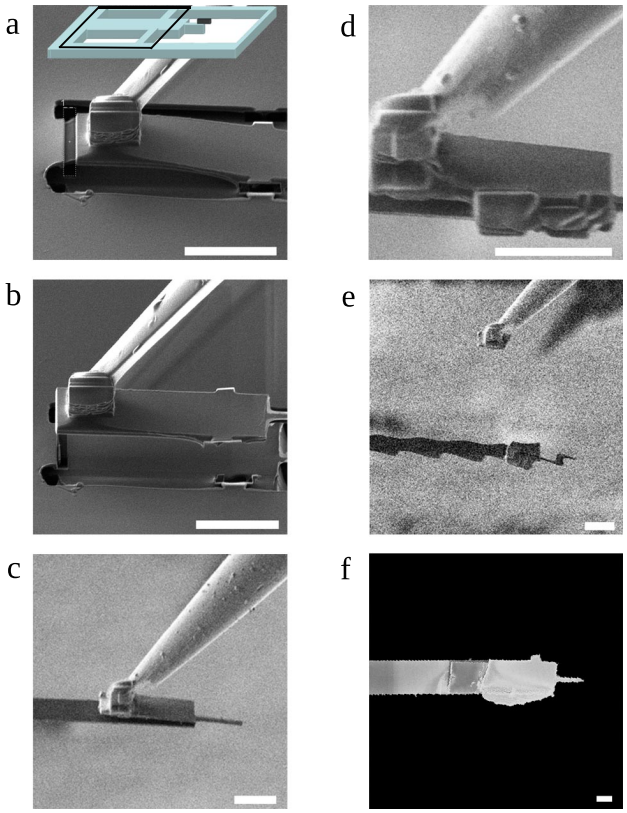

Figure 3.5: Ion-beam side-view (panels (a-e)) and SEM top-view (panel (f)) images detail the original magnet-tipped chip lift-out and cantilever attachment procedure using a dual beam FIB instrument. The inset in panel (a), which includes a schematic of the chip device layer from Figure 3.2(c), indicates the chip orientation, and the box details the visible region of the chip in the subsequent images. The process includes: (a) adhesion of the probe tip to the magnet-tipped chip by FIB deposition of platinum; (b) milling of the chip's support tethers and lift-out of the chip; (c) positioning of the chip over the cantilever's leading edge and bringing the chip into contact with the cantilever; (d) adhesion of the chip to the cantilever by FIB deposition of platinum deposition; (e) milling and removal of the probe tip; and (f) completion of the chip-on-cantilever process. The serial attachment process requires approximately 1.5 hours per fabricated chip-on-cantilever assembly, with an additional 0.5 hour for sample loading and unloading from the chamber. All scale bars represent 5 µm.

leading-edge silicon finger had to be carefully chosen in order to prevent stiction. The need for support tethers can be seen in Figure 3.6(a), which shows that 15 µm long chips without tethers snapped into contact with the underlying substrate. The silicon finger at the leading edge incurred stiction and curling if it was 5 µm long (Figure 3.6(b)), but was stiction-free even without critical point drying for short finger lengths of 2-3 µm (Figure 3.2(c)). Slits that were too wide resulted in stiction, whereas slits that were too narrow did not provide room for lateral motion during the FIB lift-out procedure. Since stiction occurred in approximately 50% of chips with slit widths of 4 µm and in all chips with slit widths wider than 6 µm, widths of 2 to 3 µm were chosen. Support tethers that were too narrow also resulted in stiction (Figure 3.6(c)), whereas support tethers that were at least 4 µm wide remained stiction-free (Figure 3.2(a-c)).

The nickel nanomagnet yield was estimated by visual inspection using an SEM (Zeiss Ultra 55 microscope); analysis of the nickel magnetization was conducted separately using cantilever frequency-shift cantilever magnetometry, and those results are included in Chapter 4. Visual analysis of the magnets was used to confirm whether (1) part or all of the magnets were missing after processing or (2) the metal had reacted to form either nickel silicide or nickel oxide. Damage would appear as either removal of the magnetic material or the transformation of crystalline nickel into "blob-like" amorphous balls, as seen for damaged nanomagnets integrated on cantilevers in Figure 2.2. It was observed that overhanging nanomagnets were present on nearly 100% of the magnet-tipped chips. Since the nickel grain structure was clearly visible (Figures 3.3(c-f)), it was concluded that the magnets had no appreciable damage due to silicidation or oxidation.

The cantilever yield for the wafer prepared for these experiments was 90.5%, with 190 out of 210 potential cantilevers remaining intact. Yields for similarly processed wafers have ranged from 50% to 90%. The FIB lift-out and attachment procedure yield was 91%, with

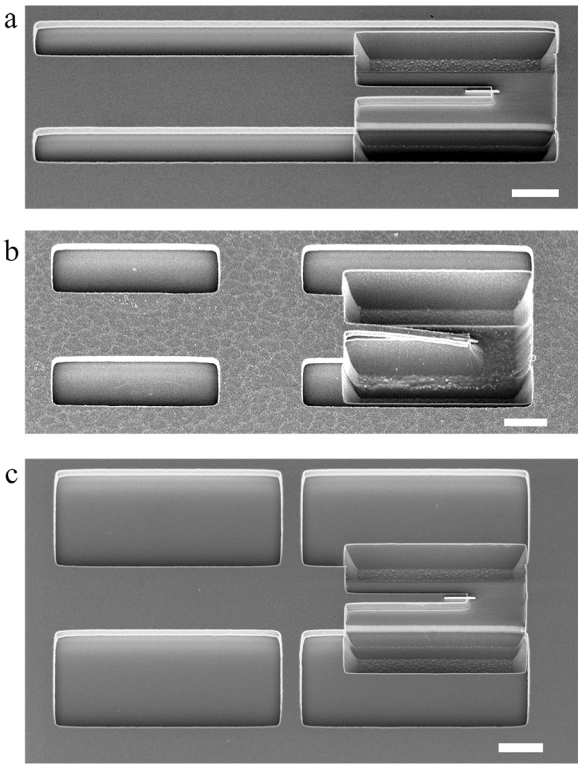

Figure 3.6: SEM images of unsuccessful alternative dimensions for the support tethers, silicon "finger" length, and slit width. Stiction was observed for magnet-tipped chips with (a) no support tethers, (b) long silicon fingers, and (c) wide slits and narrow support tethers. For comparison, free-standing chips have an observable gap between the finger and the substrate, as shown in Figure 3.3. All scale bars represent 2 µm.

only one failure out of eleven attempts (caused by a crack in the chip silicon that propagated during lift-out). After FIB manipulation, the cantilever quality factors remained high, implying that the cantilevers were not damaged by the FIB processing. Cantilever quality factors were measured for six magnet-on-cantilever assemblies and ranged from 41,000 to 94,000 at 4.2 K and 10^{-6} mbar (shown in Table 4.1 in Chapter 4); these Q's are consistent with previously reported values for non-FIB processed cantilevers [68, 81].

3.6 Switching to Cobalt Magnets

Although nickel nanomagnets have been used in MRFM experiments to detect electron spin resonance [81], switching to a magnetic material with a significantly higher saturation magnetization would increase the tip-field gradient produced by the nanomagnet and greatly enhance the signal-to-noise ratio in MRFM experiments [48]. For instance, it would be highly desirable to switch from nickel, which has a saturation magnetization of only $\mu_0 M_{sat} = 0.6$ T, to cobalt, which has a three-times-larger saturation magnetization of $\mu_0 M_{sat} = 1.8$ T. Previous efforts to fabricate cobalt nanomagnets by e-beam lithography were unsuccessful [81]. By modifying the nanomagnet-tipped chip fabrication protocol detailed in Section 3.2 to not exceed temperatures of 115°C, cobalt nanomagnets defined by e-beam lithography can be fabricated for the first time. The importance of reducing the processing temperature can be observed in Figure 3.7; it can be seen that cobalt nanomagnets that were exposed to temperatures of 170°C during resist baking were damaged significantly (Figure 3.7(a)), whereas cobalt exposed to reduced temperatures of only 115°C remained intact (Figure 3.7(b)).

Cobalt nanomagnet-tipped chips were fabricated using the same basic procedure outlined in Section 3.2, except that the temperature never exceeded 115°C once the nanomagnets were deposited. Etch slits were defined in the SOI wafer's device layer and the resulting chips

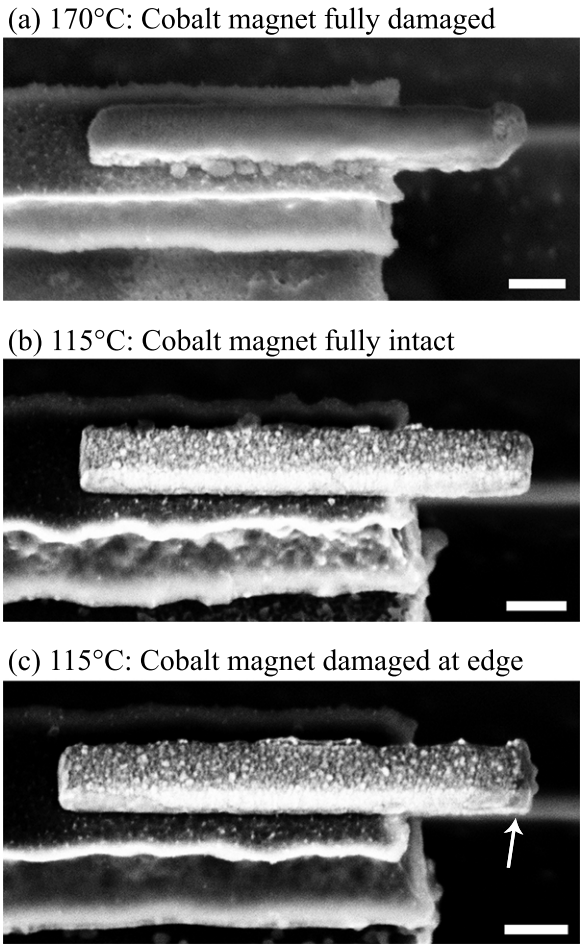

Figure 3.7: SEM images of overhanging cobalt nanomagnets. (a) An uncapped cobalt nanomagnet that was damaged by exposure to 170°C temperatures. (b) A fully intact, platinum-coated nanomagnet that was undamaged by processing at a reduced temperature of 115°C. (c) A cobalt nanomagnet from the same wafer as (b) that was damaged at the leading 20 nm of the nanomagnet, as denoted by the arrow. All scale bars represent 200 nm.

were released using 6:1 BOE prior to deposition of the nanomagnets. The magnets were defined using e-beam lithography in a bilayer resist of 50 nm of 950,000 MW PMMA on 550 nm of 495,000 MW PMMA, and the metal was deposited by e-beam evaporation. The nanomagnets were prepared by depositing a titanium adhesion layer (deposited at 1.5 Å/sec), cobalt (2.9 Å/sec), and a platinum capping layer (1.2 Å/sec). Relative metal thicknesses were measured during deposition by a quartz crystal microbalance, and the combined thickness of the Ti/Co/Pt film was measured after fabrication by atomic force microscopy (AFM). For the cobalt nanomagnet studied by frequency-shift cantilever magnetometry in Section 4.4 and used to detect NMR signal from a polystyrene film in Chapter 5, the layer thicknesses were 4.0 ± 0.2 nm of titanium, 79.2 ± 4.7 nm of cobalt, and 8.0 ± 0.5 nm of platinum. Silicon under the leading 300 nm of the magnets was removed by patterning U-shaped holes [81, 82] in a layer of 700 nm thick, 495,000 MW PMMA resist; cobalt oxidation was prevented at this step by baking the PMMA at only 115°C for 40 minutes (in Section 3.2, the resist was baked at 170°C for 20 minutes). The inside edge of the U-shaped hole was patterned to be offset from the nanomagnet leading edge by 50 nm. The silicon under the U-shaped hole was isotropically etched using SF_6:O_2 plasma.

Although yield as determined by SEM visual analysis was generally excellent for the cobalt nanomagnet-tipped chips, one problem was observed. For some overhanging nanomagnets, approximately 20 nm of cobalt at the leading edge was removed between the deposition of the nanomagnets and the end of the process. The damage was not consistent throughout a wafer; undamaged magnets ((Figure 3.7(b)) and damaged magnets ((Figure 3.7(c)) were interspersed on the same 1 mm wide die. It is interesting to note that although the leading edge of the nanomagnet was damaged, as indicated by the arrow in Figure 3.7(c), the back and side edges of the nanomagnet remained intact. Although quantitative yields were not recorded, estimates indicate that 10% to 50% of magnets per die incurred this leading-edge damage.

The source of the cobalt nanomagnet leading-edge damage is not fully understood. Since the damage occurred at only one edge of the magnet, it is not consistent with oxidation or silicide formation. Damage could have been due to an interaction with the SF_6:O_2 plasma, but then it is not understood why only some of the nanomagnets were effected. Since the magnets were capped with 10 nm of platinum and covered by PMMA resist, which left only the undamaged titanium adhesion layer exposed to the plasma, it is also difficult to see how the plasma could have reacted with the cobalt. The source of this damage will remain an open field of investigation. However, even magnets with this leading edge damage have been found to be suitable for high-sensitivity MRFM measurements. In fact, a nanomagnet with 10 to 20 nm of damage at the leading edge produced a tip-field gradient that is comparable to the tip employed in the 4 to 10 nm resolution imaging experiment of Ref. 12 (see Chapter 5 and Ref. 58).

3.7 Improvements to the Chip Design

3.7.1 Side Tabs Added to Magnet-Tipped Chips

During FIB lift-out of the original rectangular magnet-tipped chips (Figure 3.5), the FIB probe needle was adhered near the base of the chip and centered with respect to the chip's width. When the chip was positioned over a cantilever, the probe needle was thus also centered directly over the cantilever. After the attachment was complete, the probe needle could only be removed by milling through the adhesion point between the chip and the needle. Often the 1 µm-wide platinum adhesion point did not mill uniformly, causing some of the silicon under the needle to be milled during extraction. Milling a small hole into the cantilever could weaken the structure and increase the bending of the cantilever at

that position. Further milling could completely mill through the adhesion point between the magnet-tipped chip and the cantilever, and would result in the removal and loss of the magnet-tipped chip. Although this step was carefully monitored and chip-on-cantilever attachment yields were almost 100%, modified chips designs were sought out to mitigate this risk of milling into the cantilever body.

For the second generation of magnet-tipped chips, a key change in the design that improved the attachment process was the addition of a "side tab" to the shape of the chip. An image of this second-generation magnet-tipped chip design is shown in Figure 3.8(a);[3] the side tab is shown at the top of the chip. The probe needle could be attached to this side tab during FIB lift-out (Figure 3.8(b-c)). After the magnet-tipped chip was attached to a cantilever, the entire side tab was milled away to cleanly separate the probe needle from the magnet-on-cantilever assembly (Figure 3.8(d)). With this improved process, no milling ever was conducted over the body of the cantilever. The process of attaching the probe needle to the tab, lifting out the chip and attaching it to a cantilever, and particularly removing the probe needle from the chip-on-cantilever assembly was faster and more straight-forward using this enhanced design.

Since these second-generation chips were larger to accommodate the addition of the side tabs, the chip shape had to have rigid structural support so that it would not incur stiction during processing. The chips were designed to have four support tethers: two tethers were located at the bottom of the magnet-tipped chip, and two more were at the top of the chip between the side tab and the surrounding silicon substrate. The tab shape was designed to provide stability both during subsequent fabrication of the suspended chips and during the FIB lift-out process, when the chip body was suspended by the probe needle attached to the tab. The yield of fabricating these second-generation chips was nearly 100%.

[3]Figure 3.8 reprinted with permission from the Supporting Information for J. G. Longenecker *et al.*, ACS Nano **6**, 9637 (2012). Copyright 2012, American Chemical Society.

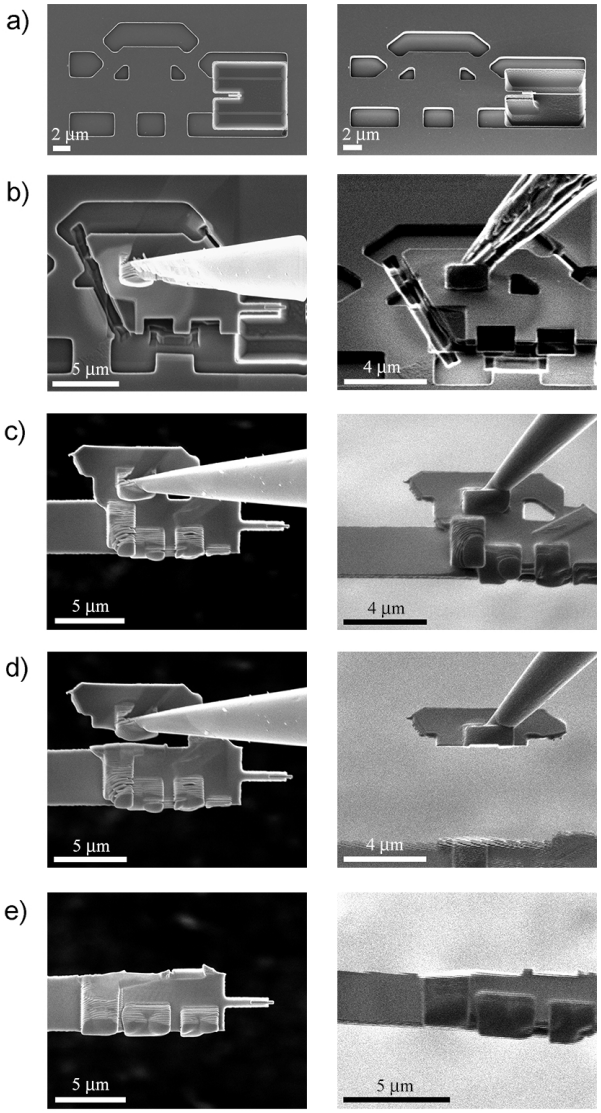

Figure 3.8: Second-generation magnet-tipped chip design and a revised FIB attachment procedure. Top-down SEM (left column) and side-on FIB images (right column) of the key steps used to remove the magnet-tipped silicon chip from the substrate [panels (a)-(b)] and attach it to the leading edge of a blank cantilever [panels (c)-(e)]. To remove the chip from the substrate, a probe needle was attached to the silicon tab connected to the chip, the support tabs were milled, and the shape of the chip was fine-tuned in order to promote superior adhesion to the cantilever by milling rectangular holes into the side of the chip and angling the back edge of the chip [panel (b)]. The chip was positioned over the leading edge of the cantilever and adhered to the cantilever by depositing FIB-assisted platinum in the rectangular holes and at the back edge of the chip [panel (c)]. The tab at the side of the chip was milled away [panel (d)] in order to cleanly separate the probe tip from the chip-cantilever assembly [panel (e)].

Concurrently with modifying the shape of the second-generation chips, steps during the FIB lift-out process to refine the chip shape in preparation for adhesion to the cantilever were introduced (Figure 3.8(b)). Specifically, two rectangular holes were added on the side of the chip and the back of the chip was tapered. Both of these adjustments provided increased surface area for the platinum to adhere the chip to the cantilever during attachment (Figure 3.8(c-e)).

A third-generation chip shape was also designed and fabricated, but has not yet been used in FIB attachment procedures. The third-generation chips were designed to be shorter, and therefore more structurally rigid, than the second-generation chips. As can be seen in Figure 3.8(b), the second-generation chips were diagonally milled during FIB lift-out so that only the rightmost two-thirds of the chips were lifted out from the substrate and attached to cantilevers. This was because it was found that the full-length, > 20 µm long second-generation chips could not be aligned vertically with the cantilevers. The chips always first touched down at the back edge of the cantilevers because the custom attonewton-sensitivity cantilevers had a slight downward bend. Since the chips were always perfectly straight, a gap was introduced between the chip and the cantilever at the chip leading edge. With short chips, this difference in angle did not lead to a significant gap at the leading edge; however, the gap became significantly wider as the chip length was increased. It was observed that chips that were less than approximately 15 µm long could regularly be vertically aligned to cantilevers with no observable gap. The third-generation chip, which is shown in Figure 3.9, was designed to meet this shortened length criterion while still retaining the side tab for easy FIB lift-out.

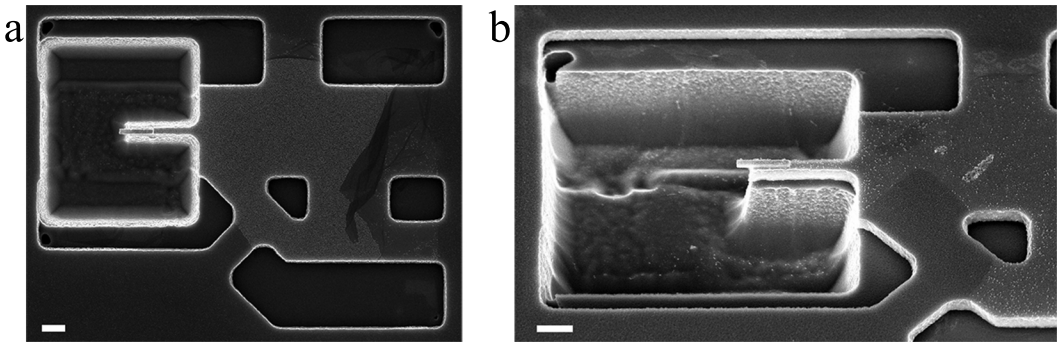

Figure 3.9: Third-generation magnet-tipped chip design. These chips were designed to be shorter than the second-generation chips, which provides extra stability and a superior shape for FIB lift-out. (a) Top-down SEM image of the full chip body. (b) Tilted and magnified SEM image of the leading edge of the magnet-tipped chip. Both scale bars represent 1 µm.

3.7.2 Fabrication of Non-Overhanging Magnet Chips

In order to assess the integrity of as-deposited nanomagnets, a simplified protocol for preparing *non*-overhanging magnets was developed. The main alteration and benefit of this process was that at the "etch slits" level of the procedure described in Section 3.2, silicon chips were defined such that one end was free-standing past the support tethers. The non-overhanging chips were pre-released in BOE so that after the magnetic material was deposited and the resist liftoff completed, the magnets could be immediately attached to cantilevers using the FIB lift-out technique. SEM images of the non-overhanging magnet chip design are shown in Figure 3.10. The fabrication of these non-overhanging magnet chips enabled the first frequency-shift cantilever magnetometry studies of nanomagnets with no post-deposition fabrication processing (Chapter 4), which was used to determine that no damage was incurred by nickel nanomagnets during the definition of the U-shaped etch pits or the etching of the silicon under the nanomagnet leading edges.

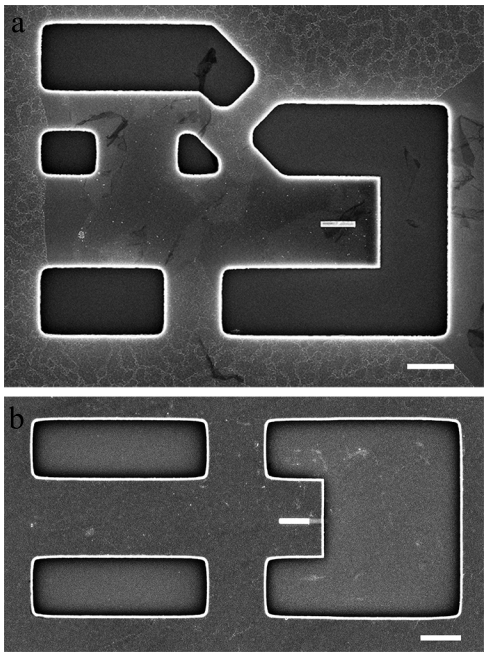

Figure 3.10: SEM images of two designs of non-overhanging magnet chips. (a) A magnet chip with a side tab and cobalt nanomagnet that was based on the third-generation magnet-tipped chip design. (b) A nickel nanomagnet on a non-overhanging chip based on the original chip design. Both scale bars represent 2 µm.

3.7.3 Incorporation of Release Chips

Release of the silicon chips from the underlying buried SiO_2 layer required an underetch of at least 2.5 µm of SiO_2. Since BOE etches SiO_2 isotropically, the SiO_2 under the silicon substrate surrounding the chips was etched back at the same rate as the SiO_2 under the chips. As the width of this suspended silicon substrate device increases, the chips become significantly more fragile. Thus, careful calibration of the BOE etch time was essential in order to make sure that the etch was stopped as soon as all chips were released.

As an easy way to identify whether the magnet-tipped chips were released, "release chips" were designed and added to each die of chips. These release chips were identical in shape to the magnet-tipped chips except that they had no tethers joining them to the surrounding silicon substrate; in other words, they were only adhered to the underlying SiO_2.

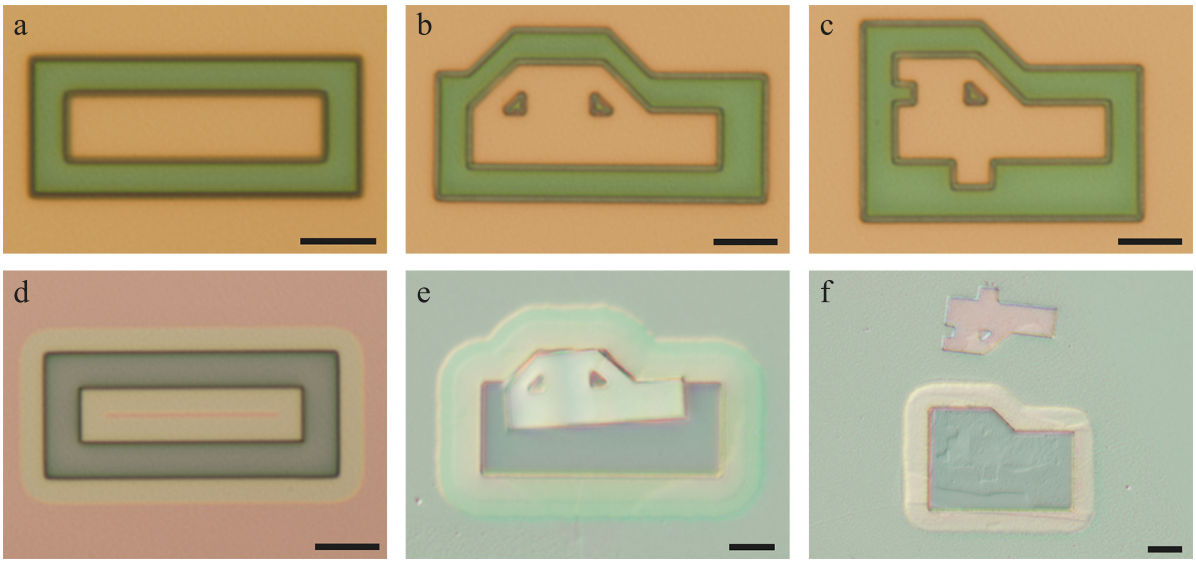

Figure 3.11: Release chips for the original design of magnet-tipped chip (left column), second-generation chip (middle), and third-generation chip (right column). Top row: Optical images of pre-released chips that were etched down to the BOX layer (green) and were still coated with resist (pink). Bottom row: Optical images at two stages of release. (d) A chip that had not been fully released – the BOX layer in the exposed regions had been etched down to the silicon (gray) and most of the SiO_2 under the rectangular chip has been etched (the freely-suspended silicon device layer appears white), but a thin strip of SiO_2 under the center of the rectangular chip had not yet been released (the device silicon layer with SiO_2 underneath appears pink). (e-f) Two examples of how the movement of the release chips after the BOX was completely underetched clearly indicates that they had been fully released. Note that the chip in panel (d) was etched by HF vapor (see Section 3.8); no images of partially-etched chips using BOE etchant were recorded. All scale bars represent 5 µm.

Therefore when the SiO_2 was completely underetched, the release chips were free to fall to the underlying handle silicon layer or to float away in the liquid BOE. When imaging a wafer to determine whether the chips were fully suspended, the release could be easily determined based on whether the release chips were still in position (not yet released) or if they had moved or were absent (fully released). Optical images of the release chips for the three different magnet-tipped chip designs before (top row) and after (bottom row) BOE etching are shown in Figure 3.11.

3.8 Chip Release by HF Vapor

In the magnet-tipped chip fabrication protocols described in Section 3.2 and Section 3.6, the silicon chips were released by BOE wet etching the BOX SiO_2 layer under the chips before the magnet deposition and silicon underetch fabrication steps. This pre-release was necessary because both nickel and cobalt are readily etched by BOE; the nanomagnets would have been completely destroyed during the 50 minute BOE wet etch required to release the chips. However, many metals, including nickel, have been reported to be resistant to hydrofluoric acid (HF) vapor etching [134]. HF vapor is a dry etchant that effectively and conformally etches SiO_2 by operating at reduced pressures with ethanol as a catalyst and nitrogen as a carrier gas. Since there is no water in the system, the corrosive anhydrous reagents that react with exposed metals, such as nickel, are avoided. Nickel in particular was found by Primaxx Inc., the manufacturer of the HF vapor etching tool used in this section, to be so unreactive to HF vapor that they coated the inside of their etching chamber with a few micrometers of nickel metal to protect against chamber corrosion [135].

The resistance of nickel to HF vapor at the nanoscale was tested by releasing nickel nanomagnet-tipped chips after the magnets were deposited. Releasing completed chips was of interest since no steps were performed on suspended chips and the chips were more stable during processing. Also, since the chips were released at the end of the process, the separate steps of defining and etching (1) the etch slits and (2) the U-shaped etch pits, as described in Section 3.2, were combined into one step conducted after the magnet definition, which eliminated six steps and one-fourth of the total processing time.

A magnet-tipped chip and magnified views of nickel nanomagnets that were released using HF vapor at the end of the process are shown in Figure 3.12. The BOX SiO_2 layer was etched at a rate of 500 Å/min for 60 minutes using HF vapor in nitrogen and ethanol carrier gases (Primaxx uEtch Single Wafer Process Module; the process was conducted at

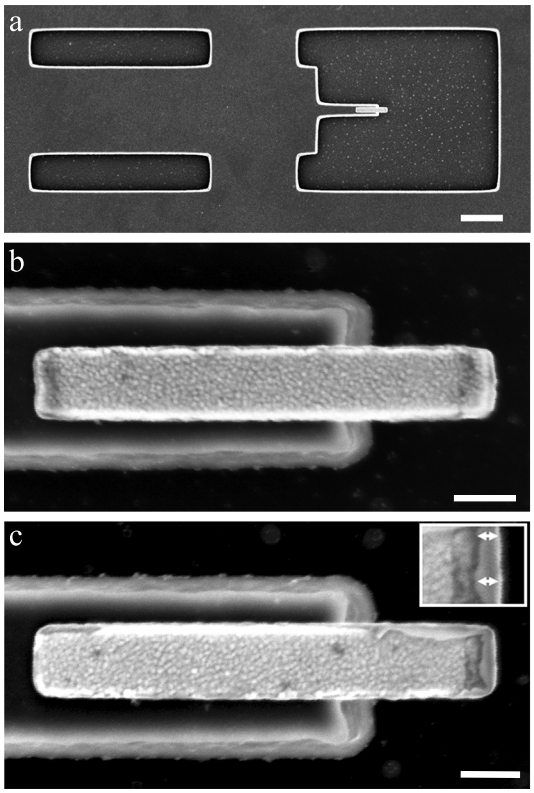

Figure 3.12: An uncapped nickel magnet-tipped chip that was released by HF vapor after magnet deposition. (a) SEM image of the released magnet-tipped chip. (b) Magnified view of a nickel nanomagnet that remained intact after HF vapor processing. (c) Magnified view of a nickel nanomagnet that was damaged during HF vapor processing. The damage to more than 20 nm of the nickel at the leading edge of the magnet is highlighted by the arrows in the inset. The scale bar in (a) represents 2 µm and the scale bars in (b) and (c) represent 200 nm.

Primaxx, Inc., in Allentown, PA, but the Cornell CNF now has an identical tool). Some of the nanomagnets remained mostly intact after processing (Figure 3.12(b)); however, it was observed that more than 20 nm of nickel at the leading edge of many of the nanomagnets was etched during the process, as indicated by the arrows in the inset in Figure 3.12(c). This result, which contradicts the findings of Ref. 134, was not well-understood. Further analysis of the damage mechanism was not conducted.

The effect of HF vapor exposure on cobalt metal was also tested using the Primaxx uEtch module (once it had arrived at the CNF). Arrays of cobalt nanomagnets (100 nm

thick) on chromium adhesion layers (5 nm thick) were defined by e-beam lithography and deposited by e-beam evaporation. After lift-off, the nanomagnets were exposed for 20 minutes to an HF vapor etch process that was calibrated to laterally etch thermal SiO_2 at a rate of 0.1 µm/min (recipe name on the CNF tool: "0.1uR7.5"). As shown in Figure 3.13, the cobalt nanomagnets were damaged significantly by the exposure to HF vapor. Large "blob-like" growths ballooned from the cobalt layers; these growths were sometimes more than 130 nm taller than the nanomagnets. Further characterization of the damaged nanomagnets was not conducted, but it was clear that HF vapor release of unprotected cobalt magnet-tipped chips after deposition was not possible.

Nickel and cobalt nanomagnets could potentially remain undamaged during HF vapor etching if they were fully encased by a material that is highly selective against HF vapor. Initial studies were undertaken to determine whether an ALD alumina (Al_2O_3) film would be a suitable protective layer; ALD tantalum oxide (Ta_2O_5) was also considered, but alumina was pursued because it could be easily removed using solvents that would not damage the nanomagnets, such as quick dips in in very dilute BOE or MIF 726 developer. Four samples of approximately 40 nm (450 loops) of alumina were prepared by ALD deposition at 110°C. The samples were exposed for 20 minutes to an HF vapor etch that was calibrated to etch thermal SiO_2 at 0.1 µm/min. As a control, one of the four samples was baked on a hot plate at 225°C for 60 seconds prior to the HF vapor exposure; this bake was recommended by Primaxx Inc. to drive off water vapor condensed on the surface of the film. The thickness of the ALD alumina was measured by ellipsometry before and after exposure to the HF vapor to determine the alumina etch rate. The etch rate for the control sample of alumina was -0.09 nm/min, and the etch rates for the other three films were -0.14 nm/min, -0.14 nm/min, and -0.04 nm/min, respectively. The negative etch rates indicate that instead of being etched, the films grew by 0.7 nm to 3 nm during the 20 minute exposure. Elemental analysis was not conducted to determine what new species were incorporated into the film, but since the

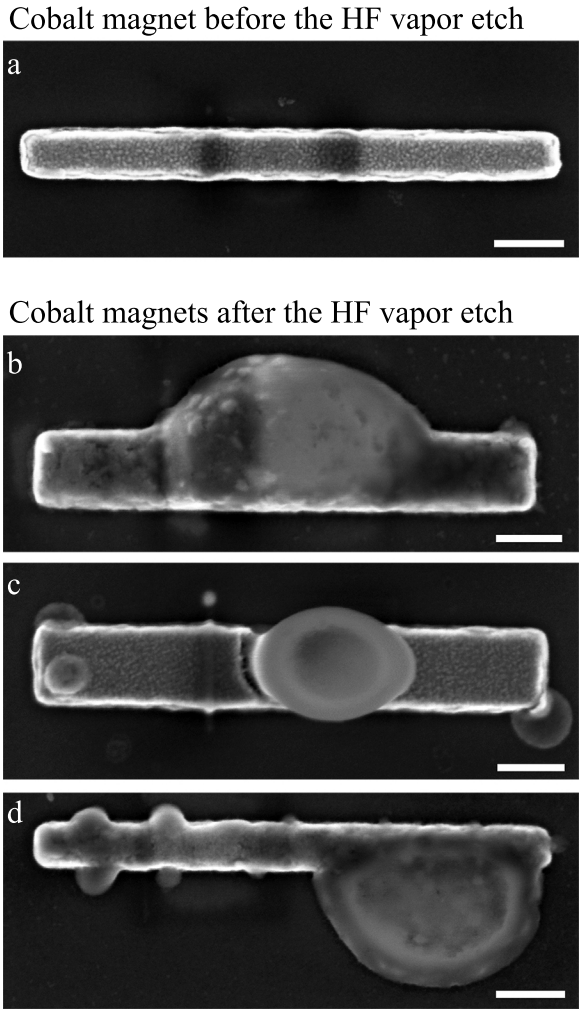

Figure 3.13: SEM images of uncapped cobalt nanomagnets that were exposed to HF vapor. (a) A cobalt nanomagnet prior to exposure to HF vapor. (b-d) Cobalt nanomagnets from the same chip as the magnet in panel (a) after they have been exposed to HF vapor for 20 minutes, which is approximately the length of exposure required for the release of magnet-tipped chips. The magnets were damaged extensively, as can be seen by the formation of growths on the nanomagnets; some of the growths were more than 130 nm taller than the cobalt nanomagnets. All scale bars represent 200 nm.

film thickness change was minimal, ALD alumina may be a suitable protective coating for the nanomagnets. If this method of capping the nanomagnets with ALD alumina would be pursued further, the challenge would be to pattern the alumina to coat the nanomagnets without covering areas of the magnet-tipped chip, including the etch slits and U-shaped holes, that need to be etched by the HF vapor. ALD alumina deposited at 110°C was observed to be removed by most liquids and could be difficult to pattern.

HF vapor etching was also considered as an alternative to BOE etching for the release of the silicon chips in the etch slit definition step, before the deposition of the nanomagnets. In the BOE release procedure of Section 3.2, it was observed that the corrosive anhydrous reagents in liquid BOE caused significantly increased surface roughness, called pitting, of the silicon device layer of some magnet-tipped chips during the 50 minute release; the extent of pitting was non-uniform over a wafer and varied extensively between wafers (Figure 3.14). Pitting of the silicon device layer led to comparable roughness of the nanomagnets deposited directly on top of the silicon. This larger-than-expected surface roughness could increase the exposed surface area of the nanomagnets, which could induce additional nickel oxidation and increase the thickness of the leading-edge damage layer.

In contrast to the effects of BOE etching, HF vapor etching of the etch slits was found to be highly selective against silicon and was not observed to alter the smooth surface of the device silicon layer. However, when this process was tested and a wafer with silicon chips that were released by HF vapor was put back into an e-beam lithography tool to align and expose the subsequent layers, it was observed that the alignment marks had disappeared; only remnant traces of metal were still present that indicated that the correct alignment mark positions had been located. It was not understood what could have caused the removal of 3 µm wide alignment marks made of 100 nm of platinum with a 5 nm thick chromium adhesion layer; chromium was not observed to be affected by HF vapor etching of nickel

nanomagnets (Figure 3.12), and platinum metal is resistant to hydrofluoric acid. Alignment marks made of different metals, such as palladium, or etched alignment marks (see Appendix C of Ref. 81) could be explored to replace the problematic platinum marks.

3.9 Discussion

The work presented in this chapter details the development of the first high-yield protocol for the fabrication of e-beam-defined nickel nanomagnets on attonewton-sensitivity cantilevers, which was achieved by fabricating the magnets *en batch* on silicon chips and attaching them serially to cantilevers by FIB manipulation. Moreover, the process for fabricating magnet-tipped chips only required a few days of processing time, compared to two weeks of processing time using the integrated magnet-on-cantilever protocol of Ref. 81.

The magnet-tipped chip protocol enabled fast prototyping of new chip designs and different magnetic materials. This rapid-prototyping capability was used to develop a revised process that eliminated high-temperature steps from the magnet-tipped chip fabrication process and led to the first successful fabrication of cobalt nanomagnets on cantilevers [58]. New chip designs were also prepared; magnet-tipped chips with side tabs made the FIB attachment process significantly more straight-forward, and the first studies of as-deposited magnets were made possible by preparing non-overhanging magnet chips.

The magnet-tipped chip fabrication process provides unprecedented flexibility for the fabrication of nanomagnets, since the cantilever processing is decoupled from the fabrication of the magnets. In future experiments, new magnetic materials, such as permalloy ($\mu_0 M_{sat}$ = 0.7 T) or sputter-deposited, amorphous CoFeB ($\mu_0 M_{sat}$ = 1.48 T) [136], could be patterned on magnet-tipped chips. The ion-beam milling that would be necessary to pattern these sputtered films would have damaged the quality factor of high-compliance cantilevers but

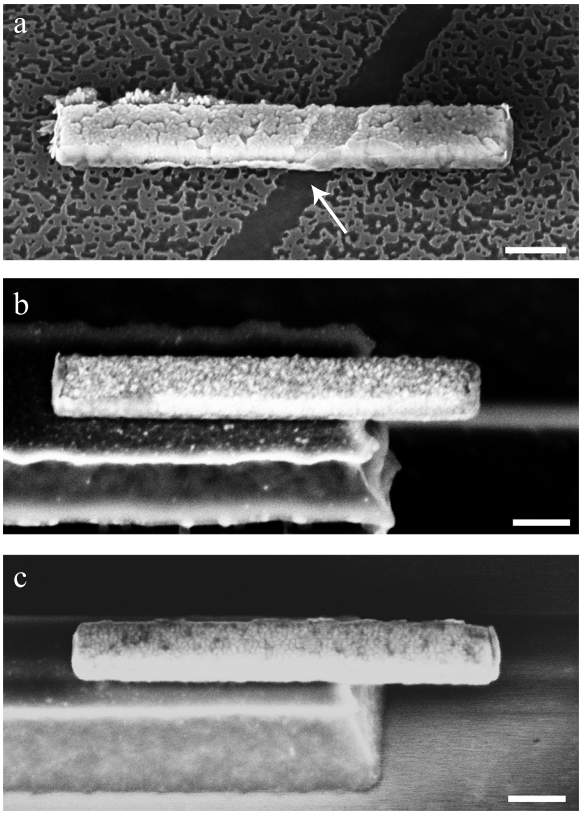

Figure 3.14: The influence of substrate roughness on the surface roughness of nanomagnets. (a) The surface roughness of a silicon substrate that was severely pitted by BOE during the chip release led to the deposition of a nanomagnet with high surface roughness. Note that the roughness of the nanomagnet corresponds to the roughness of the substrate; the nanomagnet surface roughness was large over the pitted silicon but was significantly less over the diagonal stripe of silicon that was not damaged (indicated by the arrow). (b) A cobalt nanomagnet on another wafer that was exposed to BOE. This silicon substrate was significantly less pitted than the substrate in panel (a), and the nanomagnet surface was correspondingly smoother. (c) A nickel nanomagnet deposited on a silicon wafer that had not been exposed to BOE. Note that the surface roughness of the nickel nanomagnet was minimal. All scale bars represent 200 nm.

could be integrated on magnet-tipped chips.

In addition to attaching nanomagnet-tipped chips to cantilevers, this chip-on-cantilever approach also represents a versatile route for affixing essentially any vacuum-compatible sample to the leading edge of a fragile, high-sensitivity cantilever. The combination batch- and serial-fabrication process could be used to attach a custom-fabricated magnetic tip onto the end of a commercial cantilever. Samples that require heat-intensive growing conditions such as carbon nanotubes [137] or samples that cannot tolerate the high-heat processing steps in cantilever fabrication such as superconducting rings [94] could also be adhered to cantilevers by this technique without needing to resolve process integration challenges.

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